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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/078,180	02/19/2002	Neil G. Morrow	TI-31574	5454

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TEXAS INSTRUMENTS INCORPORATED  
P O BOX 655474, M/S 3999  
DALLAS, TX 75265

EXAMINER
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CLEARY, THOMAS J

ART UNIT	PAPER NUMBER
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2111

DATE MAILED: 04/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/078,180

Applicant(s)

MORROW, NEIL G.

Examiner

Thomas J. Cleary

Art Unit

2111

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 31 January 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 8 and 15-17 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 8 and 15-17 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 19 February 2002 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## **DETAILED ACTION**

### ***Claim Rejections - 35 USC § 103***

1. Claims 8 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over the National Semiconductor DS92LV222A Two Channel Bus LVDS MUXed Repeater ("222A Repeater"), as described in the National Semiconductor Datasheet for said DS92LV222A Repeater and the MoSys Multibank DRAM ("MDRAM") as described by MoSys Preliminary Information Document "MD904 to MD920, ½ to 2½ Mbyte Multibank DRAM (MDRAM) 128Kx32 to 656Kx32."

2. In reference to Claim 8, the 222A Repeater teaches a system for extending a signal path of a host bus comprising: a first repeater portion connected to a first segment of the host bus (See 'Connection Diagram' and 'Block Diagram' on Page 1); a second repeater portion connected to a second, non-hierarchical segment of the host bus remote from the first segment of the host bus (See 'Connection Diagram' and 'Block Diagram' on Page 1), where the first and second portions of the repeater are connected by a serial link (See 'Block Diagram' on Page 1), wherein at least one of the repeater portions further comprises: an interface to the first bus segment (See 'Connection Diagram' and 'Block Diagram' on Page 1); a link translation layer connected to the transaction queue to translate incoming transactions from the host bus into serial streams to be sent over a serial link (See element 'R0' in 'Block Diagram' on Page 1)

further comprising a transaction decode circuit connected to the interface to the first bus segment to determine which transactions on the first bus to accept and pass on over the serial link (See element 'R0' and signal 'RSEL' in 'Block Diagram' on Page 1). The 222A Repeater does not teach a transaction queue with a data buffer connected to the interface. The MDRAM teaches a bus repeater having a FIFO, which is equivalent to a data buffer, connected to the interface (See Figure 1 and Paragraph 2 on Page 1).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the data buffer of the MDRAM in the 222A Repeater, resulting in the invention of Claim 8, in order to guarantee accurate I/O timing (See Column 1 Paragraph 5 on Page 2 of the MoSys Preliminary Information Document).

3. In reference to Claim 15, the 222A Repeater and the MDRAM disclose the limitations as applied to Claim 8 above. The 222A Repeater further discloses that the serial link is an LVDS link (See 'General Description' and Bullet 1 of 'Features' on Page 1).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the data buffer of the MDRAM in the 222A Repeater, resulting in the invention of Claim 15, in order to guarantee accurate I/O timing (See Column 1 Paragraph 5 on Page 2 of the MoSys Preliminary Information Document).

4. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over the 222A Repeater and MDRAM as applied to Claim 8 above, and further in view of US Patent Application Publication Number 2003/0065869 to Balay et al. ("Balay").

5. In reference to Claim 16, the 222A Repeater and MDRAM teach the limitations as applied to Claim 8 above. The 222A Repeater does not teach that the host bus is a PCI bus. Balay teaches connecting PCI buses together by converting the PCI signals on the first bus to a high speed serial connection such as LVDS, communicating the signals over the high speed serial connection, and converting the signals back to PCI to be transmitted on the second bus (See Figures 1 and 2 and Page 2 Paragraphs 24-26).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a 222A Repeater with the data buffer of MDRAM to connect the PCI buses of Balay, resulting in the invention of Claim 16, because PCI is a standard implementation which provides a well-standardized backplane structure that allows different line cards to be connected (See Page 1 Paragraphs 4-5 of Balay).

6. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over the 222A Repeater and MDRAM as applied to Claim 15 above, and further in view of The Low Pin Count (LPC) Interface Specification from Intel ("Intel 1997").

7. In reference to Claim 17, the 222A Repeater and MDRAM teach the limitations as applied to Claim 15 above. The 222A Repeater and MDRAM do not teach that the host bus is an LPC (Low Pin Count) bus as defined by Intel 1997. Intel 1997 teaches the use of a serialized LPC bus (See Page 1 Chapter 1 and Page 6 Section 4.2).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a 222A Repeater with the data buffer of MDRAM to connect the LPC buses of Intel 1997, resulting in the invention of Claim 17, because LPC has a reduced cost, allows synchronous design, is transparent and thus does not require special drivers or configuration, and supports desktop and mobile implementations (See Page 1 Section 1.1 of Intel 1997).

### ***Response to Arguments***

8. Applicant's arguments with respect to claims 8 and 15-17 have been considered but are moot in view of the new ground(s) of rejection.

9. Applicant has argued that signal RSEL does not control the 222A Repeater to determine which transactions on a single bus segment to accept and pass on over a serial link. Signal RSEL is used to turn on element R0, which allows signals to pass, and to turn off element R0, which prevents signals from passing. RSEL determines which data on bus RI0 (consisting of lines RI0+ and RI0-) to pass through. Data can be present on bus RI0 both when element R0 is on and when element R0 is off. If it is determined that the data on bus RI0 is to pass through, RSEL turns on element R0. If it is determined that the data on bus RI0 is not to pass through, RSEL turns off element R0. As such, contrary to Applicant's assertion, RSEL is determining which transactions are accepted and passed on over the serial link. Applicant has further argued that

RSEL controls the 222A Repeater to determine from which of two buses data is to be provided to an output buffer. The Examiner notes that the claims do not prohibit other link transactions layers from being connected to the serial link, nor do the claims require that only one link transaction layer be connected to the serial link. As shown above, R0 determines which transactions on bus R10 are accepted and passed on over the serial link. The Examiner further notes that although the specification refers to decoding which address ranges should be forwarded to the other segment (See Page 6 Lines 1-11), the claims do not recite this limitation. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

### ***Conclusion***

10. The following prior art made of record and not relied upon is considered pertinent to Applicant's disclosure: US Patent Number 5,283,781 to Buda et al.; US Patent Number 5,999,389 to Luebke et al; and US Patent Number 6,363,085 to Samuels.

Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Thomas J. Cleary whose telephone number is 571-272-3624. The Examiner can normally be reached on Monday-Thursday (7-3:30), Alt. Fridays (7-2:30).

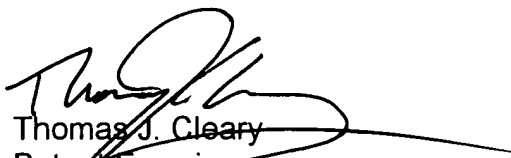
If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Mark H. Rinehart can be reached on 571-272-3632. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TJC



MARK H. RINEHART  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2100



Thomas J. Cleary  
Patent Examiner  
Art Unit 2111